Exhibit 6

iSmartgate Cameras (see product list at end of chart for models) Infringement of the '242 patent	
Claim 1	**Evidence**
1. A method of processing imaging signals, the method comprising:	The iSmartgate camera performs a method of processing imaging signals. For example, the iSmartgate camera includes an image processor that processes imaging signals. The image processor processes imaging signals that are received from an image capturing system via an interface of the camera.
receiving image data from an imaging array;	The iSmartgate camera receives image data from an imaging array. For example, the image capturing system includes a CMOS image sensor that includes an imaging array. The imaging array produces image data when exposed to an image. The interface of the iSmartgate camera receives the image data from the imaging array.
storing the image data in a FIFO memory;	The iSmartgate camera stores the image data in a FIFO memory. For example, the interface includes a FIFO memory for storing image data. The image data received from the imaging array is stored in the FIFO memory by the interface.
updating a FIFO counter to maintain a count of the image data in the FIFO memory in response to memory reads and writes;	The iSmartgate camera updates a FIFO counter to maintain a count of the image data in the FIFO memory in response to memory reads and writes; For example, the interface includes a FIFO counter to maintain a count of the image data, or "fill level", that is stored in the FIFO memory. When a unit of image data is written to the FIFO memory, the count of the FIFO counter is incremented. When a unit of image data is read from the FIFO memory, the count of the FIFO counter is decremented.
comparing the count of the FIFO counter with a FIFO limit;	The iSmartgate camera compares the count of the FIFO counter with a FIFO limit. For example, the interface includes a FIFO

	limit which it compares to the FIFO count to determine if the amount of image data in the FIFO memory is at a "fill level" that will require the interface to take an action.
generating an interrupt signal to request a processor to transfer image data from the FIFO memory in response to an interrupt enable signal being valid and the count of the FIFO counter having a predetermined relationship to the FIFO limit; and	The iSmartgate camera generates an interrupt signal to request a processor to transfer image data from the FIFO memory in response to an interrupt enable signal being valid and the count of the FIFO counter having a predetermined relationship to the FIFO limit. For example, the interface includes a processor for performing operations to transmit image data to the image processor. The servicing of interrupts by the processor can be enabled or disabled. When the servicing of interrupts from the FIFO memory is enabled and the count of the FIFO counter has a predetermined relationship to the FIFO limit, the interface generates an interrupt signal. The interrupt signal represents a request for the processor to transfer image data from the FIFO memory.
transferring image data from the FIFO memory to the processor in response to the interrupt signal.	The iSmartgate camera transfers image data from the FIFO memory to the processor in response to the interrupt signal. For example, when the processor receives the interrupt signal, the processor transfers the image data from the FIFO memory to the processor, which transmits the image data to the image processor for processing.

iSmartgate Cameras (see product list at end of chart for models) Infringement of the '242 patent	
Claim 8	**Evidence**
8. A method of processing imaging signals, the method comprising:	The iSmartgate camera performs a method of processing imaging signals. For example, the iSmartgate camera includes an image processor that processes imaging signals. The image processor processes imaging signals that are received from an image capturing system via an interface of the

	camera.
receiving image data from an imaging array;	The iSmartgate camera receives image data from an imaging array. For example, the image capturing system includes a CMOS image sensor that includes an imaging array. The imaging array produces image data when exposed to an image. The interface of the iSmartgate camera receives the image data from the imaging array.
storing the image data in a FIFO memory;	The iSmartgate camera stores the image data in a FIFO memory. For example, the interface includes a FIFO memory for storing image data. The image data received from the imaging array is stored in the FIFO memory by the interface.
updating a FIFO counter to maintain a count of the image data in the FIFO memory in response to memory reads and writes;	The iSmartgate camera updates a FIFO counter to maintain a count of the image data in the FIFO memory in response to memory reads and writes; For example, the interface includes a FIFO counter to maintain a count of the image data, or “fill level”, that is stored in the FIFO memory. When a unit of image data is written to the FIFO memory, the count of the FIFO counter is incremented. When a unit of image data is read from the FIFO memory, the count of the FIFO counter is decremented.
comparing the count of the FIFO counter with a FIFO limit;	The iSmartgate camera compares the count of the FIFO counter with a FIFO limit. For example, the interface includes a FIFO limit which it compares to the FIFO count to determine if the amount of image data in the FIFO memory is at a “fill level” that will require the interface to take an action.
generating, in response to the count of the FIFO counter having a predetermined relationship to the FIFO limit, a bus request signal to	The iSmartgate camera generates, in response to the count of the FIFO counter having a predetermined relationship to the FIFO limit, a bus request signal to request a bus arbitration unit to grant access to an output bus. For example, the interface includes a bus arbitration unit and an output bus to which the image processor is connected. When the count

request a bus arbitration unit to grant access to an output bus; and	of the FIFO counter has a predetermined relationship to the FIFO limit, the interface generates a bus request signal. The bus request signal represents a request for the bus arbitration unit to grant the interface access to the output bus.
transferring image data from the FIFO memory to the output bus in response to receiving a grant signal from the bus arbitration unit.	The iSmartgate camera transfers image data from the FIFO memory to the output bus in response to receiving a grant signal from the bus arbitration unit. For example, after the bus arbitration unit receives the bus request signal it generates a grant signal that gives the interface access to the output bus. Upon receiving the grant signal, the image data is transferred from the FIFO memory to the output bus for processing by the image processor.

Product List

iSmartgate Doorbell
iSmartgate Indoor Camera
iSmartgate Outdoor Camera

References

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[4] Amazon: iSmartgate Outdoor Camera
https://www.amazon.ca/ismartgate-Outdoor-Camera-1080p-Surveillance/dp/B08DV9ST4B/ref=sr_1_8?keywords=ISMARTGATE&qid=1638400031&sr=8-8